FIELD PLATE STRUCTURE FOR HIGH VOLTAGE DEVICES

RELATED APPLICATION

[0001] This application is based on and claims benefit of United States Provisional Application No. 60/462,562, filed on April 11, 2003, entitled Three Layer Field Plate Structure for 650V High Voltage Devices, to which a claim of priority is hereby made.

BACKGROUND OF THE INVENTION

[0002] The breakdown voltage of a semiconductor device having a PN junction is limited by the breakdown voltage of the PN junction itself. The practical maximum breakdown voltage of a PN junction is actually lower than its theoretical breakdown voltage. The discrepancy between the actual and the theoretical breakdown voltage is in part due to strong electric fields at the periphery of the PN junction itself. At this periphery, there is a transition between the electric field within the semiconductor material and the electric field in the surrounding material such as the surrounding dielectric material.

[0003] To reduce the intensity of the electric field in high electric field regions in high voltage semiconductor devices passivation structures are typically used. The purpose of the passivation structure is to provide a transition between the high electric field area near the PN junction to an area of lower potential. A passivation structure essentially reduces the electric field intensity by spreading the field lines to reduce field crowding near the PN junction thereby reducing the electric field gradient.

[0004] A known passivation structure is a field plate. A conventional field plate is comprised essentially of a relatively thick field oxide which resides over the semiconductor die and a conductive layer residing over the field oxide.

[0005] Field plates are well known for use with lateral conduction MOSFETs in CMOS technology and for other semiconductor devices to reduce high electric field gradients at the surface of the semiconductor die.

[0006] The industrial demand for cost-effectiveness is causing the designers to design semiconductor devices with smaller features. Thus, for example, in lateral conduction MOSFETs, as the photolithography line width is decreased, the field oxide thickness also decreases. As a result, for example, in 0.35 micron CMOS technology, the initial breakdown voltage of high voltage (600 volts and higher) devices with conventional multiple floating field plate ("MFETP") structures is decreased to below 600 volts because of the high electric field concentration on the oxides under the field plates. The decrease in the breakdown voltage is due to the reduction in the thickness of the field oxide.

[0007] It would be desirable to provide a field plate arrangement for lateral high voltage, low on resistance MOSFET devices with less sensitivity to surface charge.

[0008] It is further desirable to have a field plate arrangement which can be integrated into high voltage devices of over about 600 volts using 0.35 micron CMOS technology.

SUMMARY OF THE INVENTION

[0009] A field plate structure according to the present invention includes a plurality of field plates arranged vertically adjacent to one another. Each field plate according to the present invention is disposed over a respective field insulation body which may be a field oxide.

[0010] In the preferred embodiment of the present invention, a lateral conduction MOSFET includes a drift region which is disposed between a source region and a drain region. A first field plate is arranged over and spaced from the drift region by a field insulation body which may be a field oxide. Disposed over the first field plate is a second field plate which is spaced from the first field plate by

another field insulation body, which may also be a field oxide. The second field plate includes a first portion and a second portion which is spaced from the first portion by a gap. A device according to the preferred embodiment may further include a third field plate disposed over the second field plate and spaced from the same by another field insulation body which may be a field oxide. The field plate also includes a first portion and a second portion which is spaced from the first portion by a gap.

[0011] In one embodiment of the present invention the first field plate extends from the gate electrode.

[0012] A field plate according to the present invention reduces the surface charge on the field insulation beneath each plate to permit the devices to withstand 650 V or more when applied in, for example, 0.35 micron CMOS.

[0013] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 schematically shows a cross-sectional view along line 1-1 in Figure 3 of a portion of a device according to the present invention viewed in the direction of the arrows.

[0015] Figure 2 graphically shows the electric field distribution along the drift region of an example of a device according to the present invention.

[0016] Figure 3 schematically shows a top plan view of a portion of a device according to the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0017] Referring to Figure 1, an LDMOS according to the present invention includes semiconductor substrate 10 of a first conductivity which has formed over a major surface thereof an epitaxially formed semiconductor layer 12 of a second

conductivity. In the preferred embodiment of the present invention, substrate 10 and epitaxially formed semiconductor layer 12 are comprised of silicon. Also, in the preferred embodiment of the present invention the first conductivity is P type, while the second conductivity is N type.

[0018] An LDMOS according to the present invention further includes body region 14. Body region 14 is formed in epitaxially formed semiconductor layer 12 and is of the first conductivity type. Source region 18 of the second conductivity type is formed and wholly contained within body region 14. Source region 18 is adjacent invertible channel region 20 in body region 14. Formed over invertible channel region 20 is a gate structure which includes gate insulation 22, and gate electrode 24. Gate insulation 22 is formed preferably from silicon dioxide and gate electrode 24 is preferably formed from conductive polysilicon.

[0019] An LDMOS according to the preferred embodiment of the present invention further includes drain region 26 which is of the second conductivity type and is formed in epitaxially formed semiconductor layer 12. Drain region 26 is spaced from body region 14 by drift region 28 in epitaxially formed semiconductor layer 12. An LDMOS according to the preferred embodiment further includes resurf region 30. Resurf region 30 is of the first conductivity type and is found in epitaxially formed semiconductor layer 12 between drain region 26 and body region 14 over at least a portion of drift region 28.

[0020] An LDMOS according to the preferred embodiment includes a field plate structure according to the present invention which is formed over resurf region 30. A field plate structure according to the present invention includes a first field plate having first portion 32 and second portion 33 spaced from its first portion 32 by gap 39. The first field plate is disposed over and spaced from resurf region 30 by first insulation layer 34. First portion 32 of the first field plate is preferably an extension of gate electrode 24 and is thus formed from the same material. Both first portion 32 and second portion 33 in the preferred embodiment are conductive polysilicon and gap 39 between them is about 60 microns wide. First insulation

layer 34 is formed preferably from a field oxide and is preferably about 0.4 microns thick at its thickest section.

[0021] A field plate according to the present invention includes a second field plate having first portion 36 and second portion 38 spaced from its first portion 36 by gap 40. The second field plate is disposed over second field insulation 41 which is preferably composed of field oxide and is preferably 1.3 microns thick at its thickest section. Thus, the second field plate is disposed over a field insulation layer that is about 1.7 microns thick. In the preferred embodiment of the present invention gap 40 between first portion 36 of the second field plate and second portion 38 of the second field plate is about 45 microns wide.

[0022] A field plate structure according to the present invention further includes a third field plate. The third field plate includes first portion 42 and second portion 44 which is spaced from first portion 42 by gap 46. In the preferred embodiment gap 46 is about 25 microns wide. The third field plate is disposed over third field insulation layer 48. Third field insulation layer 48 is preferably 1.4 microns thick at its thickest section and composed of field oxide.

[0023] In the preferred embodiment of the present invention, second portion 44 of the third field plate is electrically connected to second portion 38 of the second field plate by an electrical connector 50. Second portion 38 of the second field plate is electrically connected to drain region 26 by an electrical connector 50. Second portion 33 of the first filed plate is electrically connected to second portion 39 of the second field plate by an electrical connector 50. Furthermore, first portion 36 of the second field plate is electrically connected to first field plate 32 by an electrical connector 50. In addition, first portion 42 of the third field plate is electrically connected to source region 20 and preferably to body region 14 by one electrical connector or a series of connectors 50.

[0024] A field plate structure according to the present invention was successfully incorporated in a 600V plus LDMOS power IC based on 0.35 micron CMOS technology. The device included a drift region of about 70 microns wide.

The following were the parameters used:

First field insulation 34	0.4 microns (at thickest section)
Second field insulation 41	1.3 microns (at thickest section)
Third field insulation 48	1.4 microns (at thickest section)
Second Field Plate	
First portion 36	1.5 microns (width over drift region)
Second portion 38	10 microns (width over drift region)
Gap 40	45 microns
Third Field Plate	
First portion 42	20 microns (width over drift region)
Second portion 44	25 microns (width over drift region)
Gap 46	25 microns

[0025] The device with the above parameters exhibited a breakdown voltage of about 650V. Figure 2 shows the electric field distribution of the device in volts/cm along the length of the drift region.

[0026] Referring now to Figure 3, the preferred embodiment of a device according to the present invention may be structured to include annular field plates, a portion of which is illustrated in Figure 3. In such a structure drain region 26 is preferably surrounded by the field plates and other features described above. For example, drain region 26 would be disposed in the center and the remaining features would annularly surround drain region 26. The curved slope of the features shown in Figure 3 is intended to illustrate the annularity of the features. The annular shape of the field plates and other features is preferably circular. Other annular shapes, however, can be adopted without deviating from the present invention.

[0027] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other

uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.